

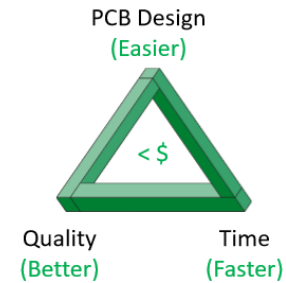
PCB Design Automation

Stackup - Build/Check/Compare

Constraint - Build/Check/Compare

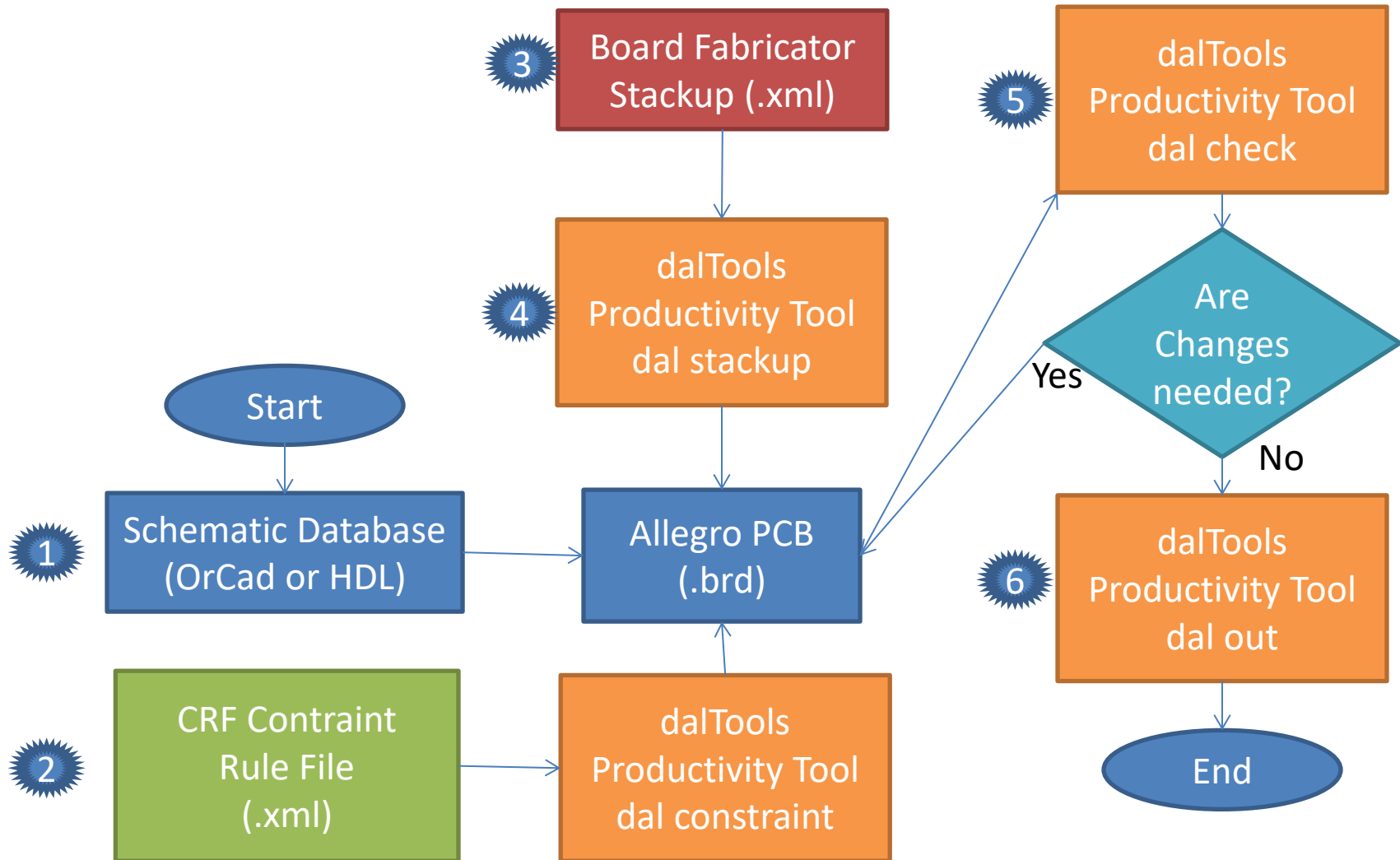
Checklist – Check/Prompt/Record

Purpose

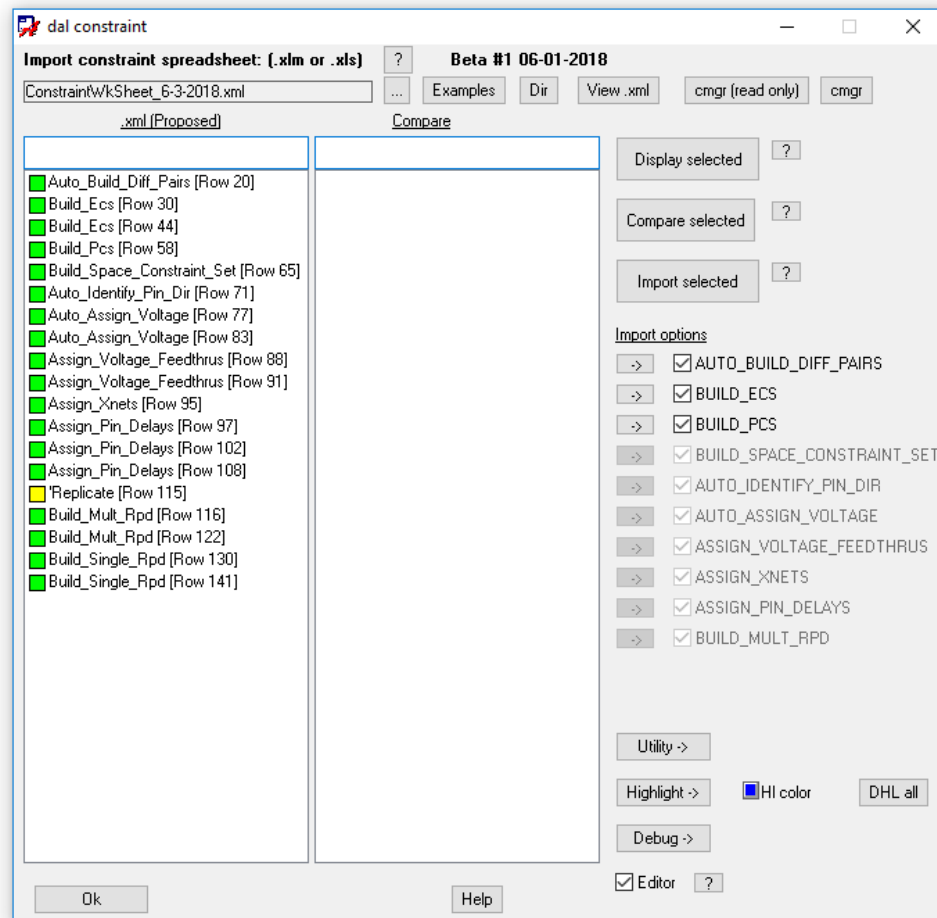


- 1. We require an easier and faster way to create and verify PCB Design layer **stackups** and impedance values. (Completed)
- 2. We require a faster and easier way to add and verify signal **constraints** in the PCB Design database. (In-work)
- 3. We require a faster and easier way to **check** the PCB Design database prior to fabrication. (In-work)

Design Automation Flow



1 dal Constraint





CRF FILE (Constraint Rule File) 1/4

B59		f	VIAS_MAX=>				
	A	B	C	D	E	F	G
1	#Helpful comments						
2	#CONSTANTS						
3	#USER ENTERED						
4	#CALCULATED						
5	#CALCULATED OR USER ENTERED....						
6							
7	#REFERENCED_BY_NAME		THESE NAMES ARE REFERENCED SOMEWHERE ELSE				
8							
9	#REFERENCED_CALCULATED_VALUES		These are the values we are calculating and can be referenced from the CRF_WORKSHEET when making the ECS rules				
10	#TBD		The definitions are a work in progress				
11							
12	COMMAND	OBJECT NAME/PARAM	VALUES				
13							
14	BUILD_STACKUP_FROM_FILE	NAME=>	BOARD_STACKUP	#THE BUILD_STACKUP_FROM_FILE COMMAND will create the stackup and the routing rules			
15		STACKUP_FILE_NAME=>	FULL_PATH/ttm_stackup.xml				
16		XML_FORMAT=>	TTM	#TTM OTHER_VENDOR_FMTS			
17		IMPEDANCE_Col=>	CALCULATED				
18							
19							
20	AUTO_BUILD_DIFF_PAIRS	DIFF_PAIR_POL_MATES=>	P:N,T:C,H:L,P:M,IBLANK:_N	#these are the Character pairs we will use to search for diff_pairs , The first character in each pair denotes the Nor			
21				#if a signal Name has a 'P' in it and we can substitute an 'N' at that position and find a matching signal name we w			
22				#similarly, if a signal name has a 'T' in it and we substitute a 'C' and find a matching signal name we call that a di			
23				#the IBLANK:_N will create a diff_pair for: diff_clk and diff_clk_n or diff1_clk and diff1_n_clk (so we only search _n s			
24				#this is an exhaustive search which finds all diff pairs, not just sig_P ,sig_N			
25							
26	#	OTHER_VALID_ECS_RULES:	VIAS_MAX=5, VIAS_MATCH=TRUE,MIN_PROP_DLY=5ps,MAX_PROP_DLY=1000ps,MIN_TOTAL_ETCH=50mil,MAX_TOTAL_ETCH=5000mil,				
27	#		TOP_MAP_MODE,TOP_VERIFY_SCHEDULE,TOP_SCHEDULE_CONTROL,STUB_LENGTH,MAX_EXPOSED,MAX_PARALLEL,LAYER_SETS				
28							
29							
30	BUILD_ECS	NAME=>	CMAC_25G	#builds a named ELECTRICAL_CONSTRAINT SET	#there should be a column on the diff_pair_tolerance_works		
31		TYPE=>	DIFF_PAIR	[SINGLE_ENDED DIFF_PAIR]			
32		ASSIGN_PCS=>	DIFF_95_OHMS				
33		GATHER_CONTROL=>	include	#[ignore include]			
34		MAX_UNCOUPLED=>	80.80808081				
35		DPA_TOLERANCE=>	6.734006734	mil			
36		DPA_MAX_LEN=>	673.4006734	mil			
37		STATIC_PHASE=>	6.734006734	mil			
38		MAX_STUB_LENGTH=>	29.5	#for back drill			
39		MEMBERS=>	MAC_QSFP				
40		MEMBERS=>	ZQSFP_MAC				
41							



CRF FILE (Constraint Rule File) 2/4

42	BUILD_ECS	NAME=>	PCIE_GEN3	#builds a named ELECTRICAL_CONSTRAINT SET	#there should be a column on the diff_pair_
43		TYPE=>	DIFF_PAIR	[SINGLE_ENDED DIFF_PAIR]	
44		ASSIGN_PCS=>	DIFF_100_OHMS		#this has to match name from imported stac
45		GATHER_CONTROL=>	include	#[ignore include]	
46		MAX_UNCOUPLED=>	252.5252525		
47		DPA_TOLERANCE=>	21.04377104	mil	
48		DPA_MAX_LEN=>	252.5252525	mil	
49		STATIC_PHASE=>	21.04377104	mil	
50		MAX_STUB_LENGTH=>	92.2	#for back drill	
51		MEMBERS=>	8G_PCIE3_RP		
52		MEMBERS=>			
53					
54					
55					
56	BUILD_ECS	NAME=>	DDR4_SE_SIGS	#builds a named ELECTRICAL_CONSTRAINT SET	
57		TYPE=>	SINGLE_ENDED	[SINGLE_ENDED DIFF_PAIR]	
58		ASSIGN_PCS=>	40OHM_SE		
59		VIAS_MAX=>	4		
60		LAYER_SETS=>	DDR4_DQ_LAYERS		
61		MEMBERS=>	c0_ddr4_addr[17:0]		
62		MEMBERS=>	c0_ddr4_{ras,cas,we,cke,odt[1:0]}		
63		MEMBERS=>	c0_ddr4_ba[1:0]		
64		MEMBERS=>	c0_ddr4_bg[1:0]		
65		MEMBERS=>	c0_ddr4_dm_dbi[8:0]		
66		MEMBERS=>	c0_ddr4_dq[71:0]		
67					
68	BUILD_PCS	NAME=>	DDR4_DIFF_SPECIAL	#builds a named PHYSICAL_CONSTRAINT SET	#there should be a column on the diff_pair_
69		ON_LAYERS=>	-12,-15	this means allowed on all routing layers except layer 12 and 15	
70		TYPE=>	DIFF_PAIR		
71		TRACE_WIDTH_PARAMS=>	We need to figure out syntax here to be able to specify trace_widths per layer... should be simplified... stackup has multiple sets of		
72					
73	BUILD_LAYER_SET	NAME=>	DDR4_DQ_LAYERS	#used to restrict routing to certain layers... good for diff pair planning and DDR planning probably	
74		LAYERS=>	L3,L5,L7		
75					
76					
77	BUILD_LAYER_SET	NAME=>	DDR4_ACTL_LAYERS	#used to restrict routing to certain layers... good for diff pair planning and DDR planning probably	
78		LAYERS=>	L9		
79					
80	BUILD_SPACE_CONSTRAINT_SET	NAME=>	CLK_DIFF_SPACE	#define SPACING_CONSTRAINT_SETS... This is a work in progress... use the 5H rule?	
81		MEMBERS=>	REF_CLK		
82		MEMBERS=>	CLK_REF		
83		LINE_TO_LINE=>	5H_RULE		
84					
85					

2 CRF FILE (Constraint Rule File) 3/4

86	AUTO_IDENTIFY_PIN_DIR	MATCH_NETS=>	MAC_QZSFP	IC_FCBGA-4344-1-S5	OUT	
87		MATCH_NETS=>	MAC_QZSFP	CNSG1X1DH4N2_223	IN	
88		MATCH_NETS=>	ZQSFP_MAC	CNSG1X1DH4N2_223	OUT	
89		MATCH_NETS=>	MAC_QZSFP	IC_FCBGA-4344-1-S5	IN	
90						
91						
92	AUTO_ASSIGN_VOLTAGE	MATCH_LIST=>	VCC_(\d+)V(\d*)	#this is a regular expression to pattern match and ca	like VCC_5V, VCC_1V8_MAC	
93		NO_MATCH_LIST=>	PG_			
94		VOLTAGE_LIST=>	\$1.\$2	#This uses the captured digits from the pattern match to build the voltage		
95						
96						
97						
98	AUTO_ASSIGN_VOLTAGE	MATCH_LIST=>	GND	#this is a regular expression to pattern match and ca	like VCC_5V, VCC_1V8_MAC	
99		NO_MATCH_LIST=>	PG_			
100		VOLTAGE_LIST=>	0.0	#This uses the captured digits from the pattern match to build the voltage		
101						
102						
103	ASSIGN_VOLTAGE_FEEDTHRU	REFDES_MATCH=>	^R\d+^B\d+^L\d+	#use this to assign voltage property to the feedthru pin of any RefDes starting with R, B o		
104		FEED_THRU_PINS=>	1-2,2-1:A-B,B-A	#this lets us assign voltages through resistors, ferrite beads and inductors if we want... w		
105						
106	ASSIGN_VOLTAGE_FEEDTHRU	SYMBOL_MATCH=>	^LS.*	#use this to assign voltage property to the feedthru pin of any symbol matching the patte		
107		FEED_THRU_PINS=>	1-2,2-1:A-B,B-A	#this lets us assign voltages through resistors, ferrite beads and inductors if we want... w		
108						
109						
110	ASSIGN_XNETS	ASSIGN_MODELS_ACROSS=>	*_AC,*_BUF			
111						
112	ASSIGN_PIN_DELAYS	SYMBOL=>	IC_FCBGA-4344-1-S5	#assigns a pin_delay file to a matching symbol		
113		FILE=>	PATH/BCOM_PIN_DELAYS.csv			
114		FILE_CONTENT_FMT=>	PIN_NUM,PIN_DLY_PS			
115		FILE_HDR_ROWS=>	(NONE,1,2,3)			
116						
117	ASSIGN_PIN_DELAYS	REF_DES=>	U157	#assigns a pin_delay file to a matching ref_des		
118		FILE=>	PATH/FPGA_PIN_DELAYS.csv			
119		FILE_CONTENT_FMT=>	PIN_NAME,PIN_DLY_PS	#note sthis could map pin_delays to pin_name instead of pin num		
120		FILE_HDR_ROWS=>	(NONE,1,2,3)			
121						
122						
123	ASSIGN_PIN_DELAYS	REF_DES=>	U1,u2,u3,u83	#assigns a pin_delay file to a matching ref_des		
124		FILE=>	PATH/CPLD_PIN_DELAYS.csv			
125		FILE_CONTENT_FMT=>	PIN_DLY_PS,PIN_NUM			
126		FILE_HDR_ROWS=>	(NONE,1,2,3)			
127						
128						



CRF FILE (Constraint Rule File) 4/4

129	#RELATIVE PROP DELAYS				
130	*REPLICATE C0_=>C0_C1_C2_C3_				
131	BUILD_MULT_RPD	c0_ddr4_dq_lanes_x4		#This will create 18 Relative propagation delay groups, one for each nibble/stb	
132		TOLERANCE=>	6ps		
133		MEMBERS=>	c0_ddr4_dq[71:0:4]	#it uses the 71:0:4 indexes to figure out how to break the signals up into groups	
134		MEMBERS=>	dpair[tc]:c0_ddr4_dqs_t[17:0:1]		
135		TARGET=>	c0_ddr4_dqs_t[17:0:1]		
136					
137	BUILD_MULT_RPD	c0_ddr4_dq_lanes_x8			
138		TOLERANCE=>	6ps		
139		TARGET=>	c0_ddr4_dqs_t[8:0:1]		
140		MEMBERS=>	c0_ddr4_dq[71:0:8]	#alternatively, this creates 9 Relative propagaion delay groups, one for each byte/stb	
141		MEMBERS=>	dpair[tc]:c0_ddr4_dqs_t[8:0:1]		
142		MEMBERS=>	dpair[tc]:c0_ddr4_dqs_t[17:9:1]		
143		MEMBERS=>	c0_ddr4_dm_dbi[8:0:1]		
144					
145	BUILD_SINGLE_RPD	c0_ddr4_actl			
146		TARGET=>	c0_ddr4_ck_t0		
147		TOLERANCE=>	20ps		
148		MEMBERS=>	c0_ddr4_addr[17:0]	#these are the name matches from the customer	
149		MEMBERS=>	c0_ddr4_{ras,cas,we,cke,odt[1:0]}		
150		MEMBERS=>	c0_ddr4_ba[1:0]		
151		MEMBERS=>	c0_ddr4_bg[1:0]		
152		MEMBERS=>	dpair[tc]:c0_ddr4_ck_t[1:0]		
153					
154					
155					
156	BUILD_SINGLE_RPD	c0_ddr4_ck_dqs			
157		TOLERANCE=>	(-450ps,1250ps)		
158		TARGET=>	c0_ddr4_ck_t0		
159		MEMBERS=>	dpair[tc]:c0_ddr4_ck_t[1:0]	#these are the name matches from the customer	
160		MEMBERS=>	dpair[tc]:c0_ddr4_dqs_t[17:0]		
161					
162	*END_REPLICATE				
163					

3 Stackup file from Fab Vendor (.xml)

[illegible]

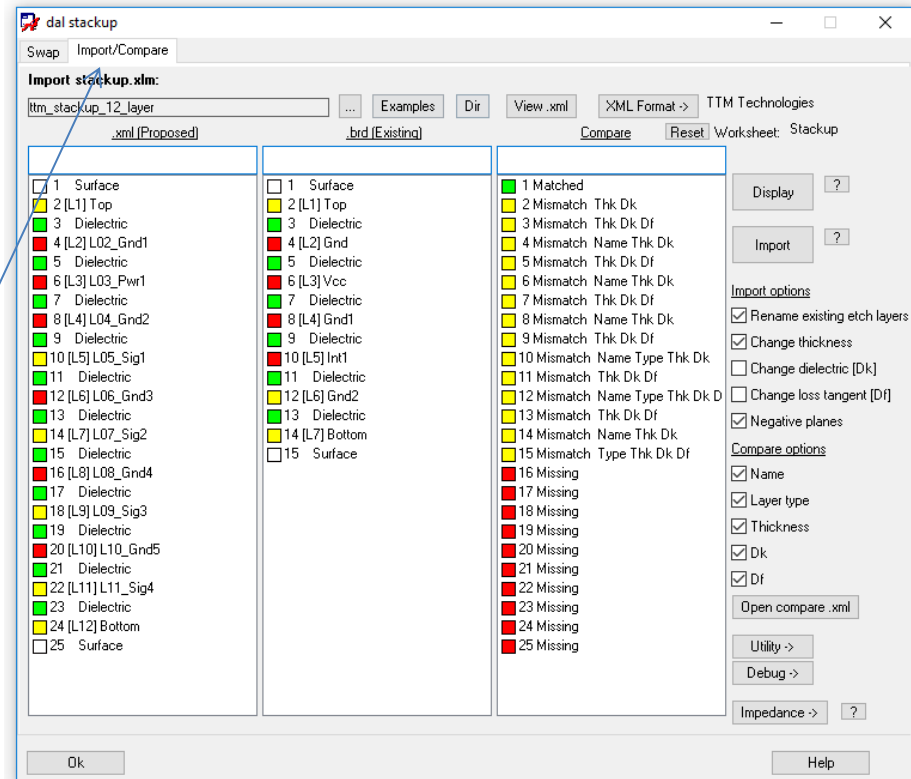


dal stackup 1/3

1. Create/compare layer names.
2. Create/compare thickness values.
3. Create/compare dielectric/loss tangent values.
4. Set/compare impedance line width and gap constraints.

New daltools feature:

Reads the
standardized
.xml file from
Fab vendor:



				Customer Stack-up		Stack-up Information						Single End			Single End			Differential			Differential		
Layer	Copper Weight	Thickness (mil)	Structure figure	Proposed Thickness (mil)	Structure	Foil type	Reference Layer	Dk	Df	Single End 50ohm ±4ohm			Single End 55ohm ±4.4ohm			Differential 90ohm ±7.0ohm			Differential 100ohm ±8.2ohm				
										Customer Design LW(mil)	Calculated LW(mil)	Calculated IMP(ohm)	Customer Design LW(mil)	Calculated LW(mil)	Calculated IMP(ohm)	Customer Design LW/SP(mil)	Calculated LW/SP(mil)	Calculated IMP(ohm)	Customer Design LW/SP(mil)	Calculated LW/SP(mil)	Calculated IMP(ohm)		
L1	Top Soldermask	0.5oz=Plate		0.60	1/3oz=Plate	HTE-PL	L1			6.00	7.90	50.00	4.88	6.40	55.00	6.25/9.75	7.7/8.3	90.00	4.00/5.50	4.5/5.0	100.00		
	101_top.art			1.97			L1												3.50/4.30	3.7/4.1	100.00		
							L1												5.00/6.80	5.3/6.5	100.00		
							L1												5.00/10.00	6.2/8.8	100.00		
							L1												6.00/10.00	6.8/10.0	100.00		
	Prepreg			4.12	R5670K_1036*2 RC70			3.06	0.002														
L2	102_gnd1.art	2oz		2.60		RTF																	
	Core			3.94	R1785V_106*2 RC71			3.68	0.019														
L3	103_pwr1.art	2oz		2.60		RTF																	
	Prepreg			3.54	R1650V_106*2 RC72			3.66	0.019														
L4	104_gnd2.art	0.5oz		0.60		HVLP																	
	Core			5.91	R5775K_1078*2 RC63			3.14	0.002														
L5	105_sig1.art	0.5oz		0.60		HVLP	L6L4			7.00	7.00	50.00	5.88	5.80	55.00	6.25/4.25	6.3/4.2	90.00	4.00/3.25	4.1/3.2	100.00		
							L6L4												5.00/4.40	5.0/4.4	100.00		
							L6L4												6.00/6.90	6.0/6.9	100.00		



Stackup 2/3

Layout Cross Section

	Subclass Name	Type	Thickness (MIL)	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (MIL)	Impedance (ohm)	Coupling Type
1		SURFACE		1	0					
2	TOP	CONDUCTOR	1.97	3.05	0.002	<input type="checkbox"/>		5.00	83.75	NONE
3		DIELECTRIC	4.12	4.5	0.035					
4	L02_GND1	CONDUCTOR	2.5	3.68	0.019	<input type="checkbox"/>		5.00	46.656	NONE
5		DIELECTRIC	3.94	4.5	0.035					
6	L03_Pwr1	PLANE	2.5	4.5	0.035	<input type="checkbox"/>	<input checked="" type="checkbox"/>			
7		DIELECTRIC	3.54	4.5	0.035					
8	L04_GND2	PLANE	0.6	4.5	0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
9		DIELECTRIC	5.91	4.5	0.035					
10	L05_SIG1	CONDUCTOR	0.6	4.5	0	<input type="checkbox"/>		5.00	49.043	NONE
11		DIELECTRIC	6.47	4.5	0.035					
12	L06_GND3	PLANE	0.6	4.5	0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
13		DIELECTRIC	5.91	4.5	0.035					
14	L07_SIG2	CONDUCTOR	0.6	4.5	0	<input type="checkbox"/>		5.00	49.043	NONE
15		DIELECTRIC	6.47	4.5	0.035					
16	L08_GND4	PLANE	0.6	4.5	0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
17		DIELECTRIC	5.91	4.5	0.035					
18	L09_SIG3	CONDUCTOR	0.6	4.5	0	<input type="checkbox"/>		5.00	49.043	NONE
19		DIELECTRIC	6.47	4.5	0.035					
20	L10_GND5	PLANE	0.6	4.5	0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
21		DIELECTRIC	5.91	4.5	0.035					
22	L11_SIG4	CONDUCTOR	0.6	4.5	0	<input type="checkbox"/>		5.00	63.197	NONE
23		DIELECTRIC	4.12	4.5	0.035					
24	BOTTOM	CONDUCTOR	1.97	1	0	<input type="checkbox"/>		5.00	87.764	NONE
25		SURFACE		1	0					

All created
automatically in 10
seconds!

Checked/Compared
automatically too.

Objects			Line Width		Neck		Min Line Spac	Primary Gap
1	Type	Name	Min mil	Max mil	Min Width mil	Max Length mil	mil	mil
4	Dsn	blank16_6	5.00	0.00	5.00	0.00	0.00	0.00
5	PCS	DEFAULT	5.00	0.00	5.00	0.00	0.00	0.00
6	PCS	50_OHM_SE	7.90:0.00:0...	7.90:0.00:0...	5.00	0.00	0.00	0.00
7	Lyr	TOP	7.90	7.90	5.00	0.00	0.00	0.00
8	Lyr	L02_GND1	0.00	0.00	5.00	0.00	0.00	0.00
9	Lyr	L03_PWR1	0.00	0.00	5.00	0.00	0.00	0.00
10	Lyr	L04_GND2	0.00	0.00	5.00	0.00	0.00	0.00
11	Lyr	L05_SIG1	7.00	7.00	5.00	0.00	0.00	0.00
12	Lyr	L06_GND3	0.00	0.00	5.00	0.00	0.00	0.00
13	Lyr	L07_SIG2	7.00	7.00	5.00	0.00	0.00	0.00
14	Lyr	L08_GND4	0.00	0.00	5.00	0.00	0.00	0.00
15	Lyr	L09_SIG3	7.00	7.00	5.00	0.00	0.00	0.00
16	Lyr	L10_GND5	0.00	0.00	5.00	0.00	0.00	0.00
17	Lyr	L11_SIG4	7.00	7.00	5.00	0.00	0.00	0.00
18	Lyr	BOTTOM	7.90	7.90	5.00	0.00	0.00	0.00
19	PCS	55_OHM_SE	6.40:0.00:0...	6.40:0.00:0...	5.00	0.00	0.00	0.00
32	PCS	90_OHM_DIFF	7.70:0.00:0...	7.70:0.00:0...	5.00	0.00	0.00	8.30:0.00:0...
33	Lyr	TOP	7.70	7.70	5.00	0.00	0.00	8.30
34	Lyr	L02_GND1	0.00	0.00	5.00	0.00	0.00	0.00
35	Lyr	L03_PWR1	0.00	0.00	5.00	0.00	0.00	0.00
36	Lyr	L04_GND2	0.00	0.00	5.00	0.00	0.00	0.00
37	Lyr	L05_SIG1	6.30	6.30	5.00	0.00	0.00	4.20
38	Lyr	Layer L05_SIG1	0.00	0.00	5.00	0.00	0.00	0.00
39	Lyr	L06_GND3	6.30	6.30	5.00	0.00	0.00	4.20
40	Lyr	L08_GND4	0.00	0.00	5.00	0.00	0.00	0.00
41	Lyr	L09_SIG3	6.30	6.30	5.00	0.00	0.00	4.20
42	Lyr	L10_GND5	0.00	0.00	5.00	0.00	0.00	0.00
43	Lyr	L11_SIG4	6.30	6.30	5.00	0.00	0.00	4.20
44	Lyr	BOTTOM	7.70	7.70	5.00	0.00	0.00	8.30
45	PCS	100_OHM_DIFF	4.50:0.00:0...	4.50:0.00:0...	5.00	0.00	0.00	5.00:0.00:0...



Stackup 3/3

A1 Num						
	A	B	C	D	E	
1	Num	Name	Line Width	Primary Gap	PCS	Type
2	1	TOP	7.9 -> 7.4		50_OHM_SE	SE
3	2	L05_SIG1	7		50_OHM_SE	SE
4	3	L07_SIG2	7		50_OHM_SE	SE
5	4	L09_SIG3	7		50_OHM_SE	SE
6	5	L11_SIG4	7		50_OHM_SE	SE
7	6	BOTTOM	7.9 -> 7.8		50_OHM_SE	SE
8						
9	8	TOP	6.4		55_OHM_SE	SE
10	9	L05_SIG1	5.8		55_OHM_SE	SE
11	10	L07_SIG2	5.8		55_OHM_SE	SE
12	11	L09_SIG3	5.8		55_OHM_SE	SE
13	12	L11_SIG4	5.8		55_OHM_SE	SE
14	13	BOTTOM	6.4		55_OHM_SE	SE
15						
16	15	TOP	7.7	8.3	90_OHM_DIFF	DIFF
17	16	L05_SIG1	6.3	4.2	90_OHM_DIFF	DIFF
18	17	L07_SIG2	6.3	4.2	90_OHM_DIFF	DIFF
19	18	L09_SIG3	6.3	4.2	90_OHM_DIFF	DIFF
20	19	L11_SIG4	6.3	4.2	90_OHM_DIFF	DIFF
21	20	BOTTOM	7.7	8.3	90_OHM_DIFF	DIFF
22						
23	22	TOP	4.5	5.0	100_OHM_DIFF	DIFF
24	23	L05_SIG1	4.1	3.2	100_OHM_DIFF	DIFF
25	24	L07_SIG2	4.1	3.2	100_OHM_DIFF	DIFF
26	25	L09_SIG3	4.1	3.2	100_OHM_DIFF	DIFF
27	26	L11_SIG4	4.1	3.2	100_OHM_DIFF	DIFF
28	27	BOTTOM	4.5	5.0	100_OHM_DIFF	DIFF
29						

Compare (.xml vs. .brd)

dal check























Customizable checklists

Analysis

Database
Circuit
Plane
Spacing
Electrical
Drill
Microvia
Backdrill
Rout
Silkscreen
Soldermask
Solderpaste
Assembly
Test
Library
Quote
Custom

Database

Severity colors: Red < Yellow. For example: Red < 4 (but not 4) Yellow 4-6 (but not 6) The Red value would be what is in the Allegro constraints and cause drcs. Yellow values are yield specific.

<input checked="" type="radio"/> On <input type="radio"/> Off Run	0  1. Unplaced symbols.....	 1	<input type="text"/>	Find Clear HL Chart Option Prio 1 ?	0/0 0.0% Unplaced symbols
<input checked="" type="radio"/> On <input type="radio"/> Off Run	0  2. Unrouted nets.....	 1	<input type="text"/>	Find Clear HL Chart Option Prio 2 ?	0/0 0.0% Unrouted nets
<input checked="" type="radio"/> On <input type="radio"/> Off Run	0  3. Unrouted connections.....	 1	<input type="text"/>	Find Clear HL Chart Option Prio ? ?	0/0 0.0% Unrouted connections
<input checked="" type="radio"/> On <input type="radio"/> Off Run	0  4. Isolated shapes.....	 1	<input type="text"/>	Find Clear HL Chart Option Prio ? ?	
<input checked="" type="radio"/> On <input type="radio"/> Off Run	0  5. Unassigned shapes.....	 1	<input type="text"/>	Find Clear HL Chart Option Prio ? ?	
<input checked="" type="radio"/> On <input type="radio"/> Off Run	0  6. Out of date shapes.....	 1	<input type="text"/>	Find Clear HL Chart Option Prio ? ?	0/0
<input checked="" type="radio"/> On <input type="radio"/> Off Run	0  7. Drc errors.....	 1	<input type="text"/>	Find Clear HL Chart Option Prio ? ?	
<input checked="" type="radio"/> On <input type="radio"/> Off Run	0  8. Waived drcs.....	 1	<input type="text"/>	Find Clear HL Chart Option Prio ? ?	
<input checked="" type="radio"/> On <input type="radio"/> Off Run	0  9. External drcs.....	 1	<input type="text"/>	Find Clear HL Chart Option Prio ? ?	
<input checked="" type="radio"/> On <input type="radio"/> Off Run	1  10. Drc up to date.....	 No	<input type="text"/>	Find Clear HL Chart Option Prio ? ?	
<input checked="" type="radio"/> On <input type="radio"/> Off Run	0  11. Online drc.....	 Off	<input type="text"/>	Find Clear HL Chart Option Prio ? ?	

☒ Perm HI color
☐ Temp HI color

Enabled drc modes

☒ Red
☐ Yellow

Import/Export ->
Reports ->
Dehighlight all

All on All off Run

0 ☐ 1. **Current**..... Find Clear HL

All the currently displayed and selected checks shown on this pane. (Ex. All Database checks)

Ok Cancel Run

0 ☐ 2. All..... Find Clear HL

Runs all the analysis mode checks in the upper left pane.

Help



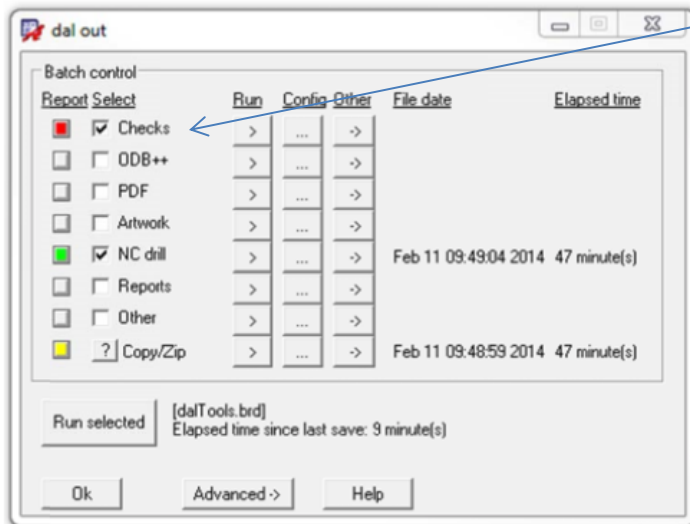
dal out

Out

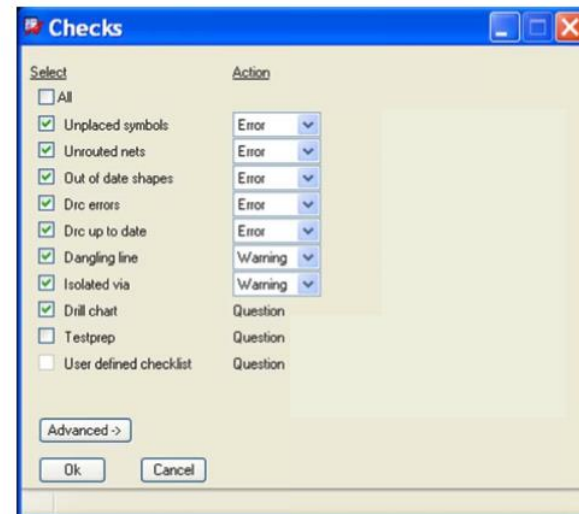
Automates the process of generating manufacturing outputs.

Features:

- ❑ Supports single click outputs of individual items or all selected items.
- ❑ All settings are stored for subsequent runs.
- ❑ Completely automates the entire extraction and release process.
- ❑ Flexible enough to meet any company's requirements.



Checks



[Database Verification](#)